Notice of Allowability	Application No. 10/671,473	Applicant(s) YAGISHITA ET AL.	
	Examiner Ly D. Pham	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 04 August 2005 and telephone interview on 22 August 2005*.

2. ☒ The allowed claim(s) is/are *4 and 7*.

3. ☒ The drawings filed on *04 August 2005* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *09/988,614* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

HUAN HOANG
PRIMARY EXAMINER

DETAILED ACTION

1. Applicant's Amendment filed August 04, 2005 has been entered. Claims 4, 7, and 10 have been entered. Claims 1 – 3 and 9 have been canceled. Claims 4 – 8 and 10 are presented for the Examination.

2. This application is in condition for allowance except the following formal matter.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ms. Michele L. Connell (reg. no. 52,763) on August 22, 2005.

The application has been amended as follows:

i. **Claims 5, 6, 8, and 10 are further canceled**.

ii. **Claims 4 and 7 are amended and rewritten** as follow.

4. A semiconductor memory device, comprising:

a plurality of subblocks, each comprising a memory array and a drive circuit located along a side of the memory array and ~~diving~~ driving lines of memory cells therein, the lines including a redundant line for repair;

an address input circuit for receiving an address signal input;

a defective line information store circuit for storing defective line information showing defective lines in the plurality of subblocks, the defective line information store circuit being shared by at least a portion of the plurality of subblocks and being located proximate to a side of one of the plurality of subblocks parallel to the defective line, wherein the plurality of subblocks which share the defective line information store circuit are located in the direction perpendicular to the lines of memory cells;

a redundant circuit, located proximate to the drive circuit of each of the plurality of subblocks and comprising a volatile storage circuit, for substituting one of the lines including the redundant line of the corresponding subblock for a defective line in that subblock according to the state of the volatile storage circuit;

common signal lines for connecting the defective line information store circuit and the redundant circuit corresponding to each subblock and for connecting the address input circuit and the drive circuit of each subblock to deliver the address signal input, the common signal lines running parallel to the drive circuit; and

a supply circuit for transferring the defective line information from the defective line information store circuit to the volatile storage circuit in the redundant circuit corresponding to each subblock via the common signal lines.

7. The semiconductor memory device according to claim 4, wherein each of the plurality of subblocks is divided into a plurality of sections, further wherein the redundant circuit performs the substitution in each of the plurality of sections.

Allowable Subject Matter

4. Claims 4 and 7 are allowed.

5. The following is an examiner's statement of reasons for allowance:

The prior arts teach a semiconductor memory device, comprising:

a plurality of subblocks, each comprising a memory array and driving lines of memory cells, the lines driving lines including a redundant line for repair;

an address input circuit for receiving an address input signal;

a defective line information store circuit for storing defective line information showing defective lines in the plurality of subblocks;

a redundant circuit comprising a storage circuit for substituting one of the lines including the redundant line of the corresponding subblock for a defective line in that subblock;

common signal lines for connecting the defective line information store circuit and the redundant circuit; and

a supply circuit for transferring the defective line information from the defective line information store circuit to the storage circuit in the redundant circuit.

However, the prior arts fail to teach the semiconductor memory device, further comprising, in combination:

the plurality of subblocks each comprising a drive circuit located along a side of the memory array;

the defective line information store circuit being shared by at least a portion of the plurality of subblocks and being located proximate to a side of one of the plurality of subblocks parallel to the defective line, wherein the plurality of subblocks which share the defective line information store circuit are located in the direction perpendicular to the lines of memory cells;

the redundant circuit comprising a volatile storage circuit and located proximate to the drive circuit of each of the plurality of subblocks for performing defective line substitution according to the state of the volatile storage circuit; wherein the redundant circuit corresponding to each subblock and for connecting the address input circuit and the drive circuit of each subblock to deliver the address input signal;

the common signal lines running parallel to the drive circuit; and

the supply circuit transferring the defective line information from the defective line information store circuit to the volatile storage circuit in the redundant circuit corresponding to each subblock via the common signal lines.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D Pham
August 22, 2005

HUAN HOANG
PRIMARY EXAMINER

Replacement Drawings
Title: SEMICONDUCTOR MEMORY DEVICE
Inventor's Name: Y. YAGISHITA et al.
Application No10/671,473
Docket No.: 107337-00053

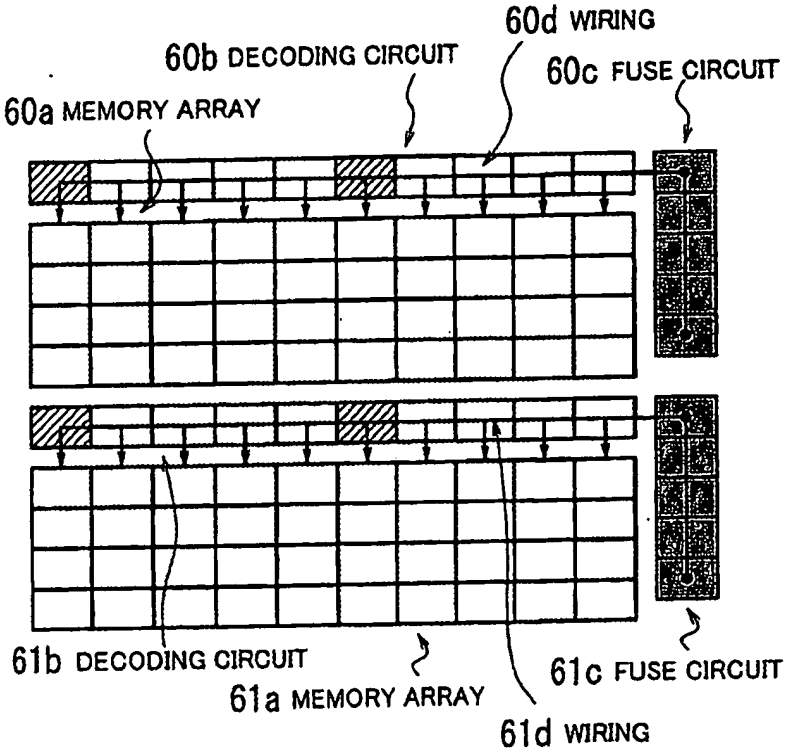

FIG. 5

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